

1/PRTS

09/762751
JC02 REC'D PCT/PTO 12 FEB 2001

5 Method of Measuring the Two-Dimensional Potential Distribution
in CMOS Semiconductor Components.

INS A1>

The invention relates to a method of measuring the two-dimensional
potential distribution in CMOS semiconductor components and of determining
10 the two-dimensional doping distribution.

INS A2>

Modern semiconductor component structures in the sub-micrometer
range require the implantation and manipulation of doping elements in silicon
semiconductor components at a lateral and vertical precision in the nm range.
15 The two-dimensional definition of such doping profiles in actual components
having a spatial resolution of this magnitude is of great significance for
optimizing physical models for the numeric simulation of the complex
fabrication processes and for the analysis of errors in real processed
components. To date, no method has become known which makes possible
20 a direct image formation of such two-dimensional doping profiles in a 324/765
transmission electron microscope (TEM). U.S. Patent 5,523,700 discloses a
method of quantitatively defining the doping profile by making use of the local
changes in capacity at the surface of a semiconductor material. Often,
because of preparation artefacts or surface segregations, the measured
25 doping distribution at the surface of a sample is not representative of
conditions within the solid body. In order to quantify a local change in
capacity as a doping distribution, it is necessary to model the local capacity.
This, however, requires elaborate electrical simulations.

30 It is an object of the invention to propose a method of measuring the
two-dimensional potential distribution in CMOS semiconductor elements and

09/762751

of determining the two-dimensional doping distribution, in which it is possible to form a direct image of the two-dimensional doping distribution and of the two-dimensional potential distribution in a transmission electron microscope.

5 The method in accordance with the invention is based upon the use of electron holography and, more particularly, electron off-axis holography in a transmission electron microscope. Electron holography permits two-dimensional measurements of the phase of an electron wave in the transmission electron microscope. The image of the phase is directly
10 proportional to the potential distribution in the spatial charge area of a pn-junctions in semiconductor structures.

 The potential distribution is measured by means of electron holography. The method in accordance with the invention is based upon
15 method steps of:

- generating a planar electron wave;
- modulating the planar electron wave as a result of transmission through a thinned cross-sectional sample of the semiconductor component;
- enlarging the modulated image wave by means of an objective lens;
- 20 - superposing the enlarged image and a planar reference wave by means of an electron bi prism;
- registering the generated electron hologram by means of a digital CCD camera, photo plates or other detector systems;
- extracting the phase of the image wave by means of a Fourier
25 analysis; and
- measuring the two-dimensional potential distribution from the phase image.

 The two-dimensional dopant distribution in CMOS structures and,
30 especially, of CMOS transistor structures is defined, and/or physical models for the simulation of the fabrication process are optimized, by comparison with

numerical simulations of fabrication process.

The characteristics of the invention will become apparent, aside from the claims, from the description and the drawings. An embodiment of the invention has been shown in the drawing and will be described in greater detail hereinafter.

Fig. 1 depicts the principle of electron holographically defining the potential distribution. Initially, a thinned cross-sectional sample is prepared. This has to be fabricated by a target preparation such that in the immediate vicinity of about 100 nm to 500 nm of the transistor to be examined there is generated a "hole" for the required planar reference wave 6 which must not be guided through the sample. The thickness of the sample near the transistor to be examined should be within an optimum range of between 50 nm and 500 nm. A planar electron wave 1 in a TEM is phase modulated by the potential distribution as it is transmitted through a thinned cross-sectional sample of the pn-junction of a CMOS transistor 2. A planar reference wave 6 is superposed on the modulated image wave 3 which has been enlarged by an objective lens 5, by means of an electron bi prism 4. The generated electron hologram 7 is registered by a digital CCD camera. Amplitude and phase of the image wave 3 are extracted by Fourier analysis. The two-dimensional potential distribution is measured on the basis of the phase image. The phase image is directly proportional to the potential distribution. Combining the image of amplitude and phase additionally permits a localized determination of the thickness of the sample.

The subsequent determination of the two-dimensional dopant distribution is carried out by adjusting the potential distribution caused by the dopant distribution to the potential distribution measured by electron holography. To this end use is made of numeric simulations of the potential corresponding to the dopant distribution.

By the present invention, a method of measuring the two-dimensional potential distribution in CMOS semiconductor components and of defining the two-dimensional dopant distribution has been set forth on the basis of a concrete embodiment. It is to be mentioned that the present invention is not
5 limited to details of the description of the embodiment as alternatives and variants are being claimed within the scope of the claims.

10

15 INS A3>

20

25

30